

PDP-1449 (Based on Form PTO-1449)

**PATENT AND TRADEMARK OFFICE
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Sheet 1 of 1

ATTORNEY DOCKET NO.

MP0039.C1

SERIAL NO.

10/786,010

APPLICANT

Pierte Roo

FILING DATE

2/26/2004

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U.S. PATENT DOCUMENTS

| Ref. Desig. | Examiner's Initials | Document Number | Date | Name | Class/ Subclass | (If appropriate) Filing Date |
|-------------|---------------------|-----------------|--------|--------------|-----------------|------------------------------|
| 1. | <i>g</i> | 6,606,489 B2 | 8/2003 | Razavi et al | — | |
| 2. | <i>g</i> | 6,870,881 | 3/2005 | He, Runsheng | — | |

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OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)

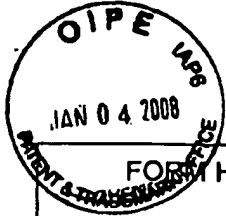
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| 1. | <i>A</i> | Stonick et al; "An Adaptive PAM-4 5-Gb/s Backplane Transceiver in 0.25-um CMOS; IEEE Journal of Solid-State Circuits, Vol. 38, No. 3, March 2003; pp. 436-443 |

Examiner:

Date Considered:

2/15/08

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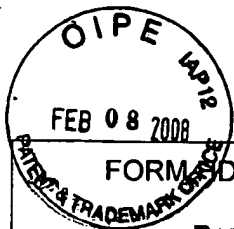
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Sheet 1 of 5

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| 4. | 9 | 6,744,931 | 06/2004 | Komiya et al. | — | |
| 5. | 9 | 6,870,881 | 03/2005 | He, Runsheng | — | |
| 6. | 9 | 6,975,674 | 12/2005 | Phanse et al. | 375/219 | |

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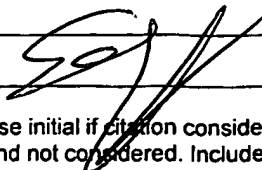
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